

What is claimed is:

1        1. A return path transmitter for use in conjunction with a local system that generates an  
2        analog RF data signal to be conveyed to a head end system, the return path transmitter  
3        comprising:

4              a sample clock generator for generating a sample clock;

5              an RF signal receiver, coupled to the sample clock generator, for receiving and  
6        converting the analog RF data signal into a first data stream of digitized RF data samples at a  
7        rate determined by the sample clock;

8              supplemental channel circuitry for providing a second data stream;

9              a multiplexor coupled to the RF signal receiver and the supplemental channel circuitry  
10      to receive the first data stream and second data stream and to output a combined data stream;  
11      and

12              an optical transmitter for converting the combined data stream into a serialized optical  
13      data signal for transmission over an optical fiber.

1        2. The return path transmitter of claim 1, including:

2              a first memory device configured to buffer the first data stream;

3              a second memory device configured to buffer the second data stream;

4              an output clock generator for generating an output clock having an associated output  
5        frequency;

6              wherein:

7              the sample clock has an associated sample rate;

8              the second data stream is generated by the supplemental channel circuitry at a rate that  
9        is less than the sample rate;

10              the multiplexor is configured to monitor a fullness level of the first memory device,  
11        output data stored in the first memory device in a first mode when the fullness level of the  
12        first memory device is more than a predefined threshold level, and to output data stored in the  
13        first memory device and data stored in the second memory device in a second interleaved  
14        mode when the fullness level of the first memory device is less than the predefined threshold  
15        level.

1        3. The return path transmitter of claim 2, wherein:

2           the supplemental channel circuitry generates maintenance data indicative of an  
3 operational state of the return path transmitter.

1     4.    The return path transmitter of claim 2, wherein:  
2           the first memory device comprises a dual ported random access memory device.

1     5.    The return path transmitter of claim 1, including:  
2           a port for receiving a third data stream from a source external to the return path  
3 transmitter, the third data stream having a data rate of at least 5 Mb/s; and  
4           merge circuitry for merging the first and third data streams into a merged data stream;  
5           wherein the multiplexor is coupled to the merge circuitry and the supplemental  
6 channel circuitry to receive the merged data stream and second data stream and to output the  
7 combined data stream.

1     6.    The return path transmitter of claim 5, including:  
2           a first memory for buffering the merged data stream;  
3           a second memory device configured to buffer the second data stream; and  
4           an output clock generator for generating an output clock having an associated output  
5 frequency;  
6           wherein:  
7           the sample clock has an associated sample rate frequency;  
8           the second data stream is generated by the supplemental channel circuitry at a rate that  
9 is less than the sample rate frequency;

10          the multiplexor is configured to monitor a fullness level of the first memory device,  
11 output data stored in the first memory device in a first mode when the fullness level of the  
12 first memory device is more than a predefined threshold level, and to output data stored in the  
13 first memory device and data stored in the second memory device in a second interleaved  
14 mode when the fullness level of the first memory device is less than the predefined threshold  
15 level.

1     7.    The return path transmitter of claim 5, wherein:  
2           the supplemental channel circuitry generates maintenance data indicative of an  
3 operational state of the return path transmitter.

1       8.     The return path transmitter of claim 7, wherein:  
2              the supplemental channel circuitry includes at least one sensor for measuring an  
3              operational parameter selected from a group consisting of temperature and supply voltage.

1       9.     The return path transmitter of claim 7, wherein:  
2              the supplemental channel circuitry includes an RF data sampler for sampling data  
3              from the first data stream to generate a set of sampled RF data and circuitry for including the  
4              sampled RF data in the second data stream.

1       10.    The return path transmitter of claim 1, wherein:  
2              the supplemental channel circuitry generates maintenance data indicative of an  
3              operational state of the return path transmitter and includes the maintenance data in the  
4              second data stream.

1       11.    The return path transmitter of claim 10, wherein:  
2              the supplemental channel circuitry includes at least one sensor for measuring an  
3              operational parameter selected from a group consisting of temperature and supply voltage.

4       12..   The return path transmitter of claim 10 wherein the supplemental channel circuitry  
5              includes an internal memory device configured to store data including at least one of a serial  
6              number, model number, date of manufacture, software revision number and hardware  
7              revision number of the transmitter, wherein the supplemental channel circuitry is further  
8              configured to include at least a portion of the data stored in the internal memory device in the  
9              maintenance data.

1       13.    The return path transmitter of claim 1, wherein:  
2              the supplemental channel circuitry includes an RF data sampler for sampling data  
3              from the first data stream to generate a set of sampled RF data and circuitry for including the  
4              sampled RF data in the second data stream.

1       14.    The return path transmitter of claim 1, wherein:

2           the supplemental channel circuitry is configured to generate the second data stream  
3           intermittently;

4           the optical transmitter includes circuitry for inserting padding words into the  
5           combined data stream so as to maintain the combined data stream at a fixed data rate.

1       15. A return path transmitter for use in conjunction with first and second local systems  
2           that generate first and second respective analog RF data signals to be conveyed to a head end  
3           system, the return path transmitter comprising:

4           a sample clock generator for generating a sample clock;

5           first and second RF signal receivers, coupled to the sample clock generator, for  
6           receiving and converting the first and second respective analog RF data signals into first and  
7           second data streams of digitized RF data samples at a rate determined by the sample clock;

8           supplemental channel circuitry for providing a third data stream;

9           a multiplexor coupled to the RF signal receivers and the supplemental channel  
10          circuitry to receive the first, second and third data streams and to output a combined data  
11          stream; and

12          an optical transmitter for converting the combined data stream into a serialized optical  
13          data signal for transmission over an optical fiber.

1       16. The return path transmitter of claim 15, including:

2           a first memory device configured to buffer the first data stream;

3           a second memory device configured to buffer the second data stream;

4           a third memory device configured to buffer the third data stream;

5           an output clock generator for generating an output clock having an associated output  
6          frequency;

7           wherein:

8           the sample clock has an associated sample rate frequency;

9           the third data stream is generated by the supplemental channel circuitry at a rate that is  
10          less than the sample rate frequency;

11          the multiplexor is configured to monitor a fullness level of the first memory device,  
12          output data stored in the first and second memory devices in a first mode when the fullness  
13          level of the first memory device is more than a predefined threshold level, and to output data  
14          stored in the first and second memory devices and data stored in the third memory device in a

15 second interleaved mode when the fullness level of the first memory device is less than the  
16 predefined threshold level.

1 17. The return path transmitter of claim 16, wherein:  
2 the supplemental channel circuitry generates maintenance data indicative of an  
3 operational state of the return path transmitter.

1 18. The return path transmitter of claim 16, wherein:  
2 the first memory device comprises a dual ported random access memory device.

1 19. A return path transmitter for use in conjunction with first and second local systems  
2 that generate first and second respective analog RF data signals to be conveyed to a head end  
3 system, the return path transmitter comprising:  
4 a sample clock generator for generating a sample clock;  
5 first and second RF signal receivers, coupled to the sample clock generator, for  
6 receiving and converting the first and second respective analog RF data signals into first and  
7 second data streams of digitized RF data samples at a rate determined by the sample clock;  
8 a data port for receiving a third data stream from a digital data source external to the  
9 return path transmitter, the third data stream having a data rate of at least 5 Mb/s; and  
10 a multiplexor coupled to the RF signal receivers and the data port to receive the first,  
11 second and third data streams and to output a combined data stream; and  
12 an optical transmitter for converting the combined data stream into a serialized optical  
13 data signal for transmission over an optical fiber.

1 20. The return path transmitter of claim 19 wherein the digital data source is an Ethernet  
2 channel.

3 21. A return path transmitter for use in conjunction with a local system that generates an  
4 analog RF data signal to be conveyed to a head end system, the return path transmitter  
5 comprising:  
6 an optical signal receiver configured to receive a digital optical signal and generate  
7 therefrom a first digitized RF data stream and a sample clock;

8           an RF signal receiver, coupled to the optical signal receiver, for receiving and  
9       converting the analog RF data signal into a second digitized RF data stream of digitized RF  
10      data samples at a rate determined by the sample clock;

11           a summing circuit for mathematically summing the first and second digitized RF data  
12      streams so as to generate a third digitized RF data stream; and

13           an optical transmitter for converting an output data stream into a serialized optical  
14      data signal for transmission over an optical fiber, the output data stream including the third  
15      digitized RF data stream.

1       22. The return path transmitter of claim 21, wherein:

2           the optical signal receiver is configured to demultiplex data within the received digital  
3      optical signal into a first digitized RF data stream and a first non-RF data stream; and

4           the return path transmitter includes:

5           a data port for receiving a second non-RF data stream from a digital data source  
6      external to the return path transmitter, the second non-RF data stream having a data rate of at  
7      least 5 Mb/s;

8           a full duplex drop and add circuit for extracting a portion of the first non-RF data  
9      stream and for replacing the extracted portion of the first non-RF data stream with the second  
10     non-RF data stream so as to generate a third non-RF data stream;

11           a multiplexor coupled to the summing circuit and the full duplex drop and add circuit  
12      to receive the third digitized RF data stream and the third non-RF data stream and to output a  
13      combined data stream; and

14           the output data stream converted by the optical transmitter includes the combined data  
15      stream.

1       23. A method transmitting data representing an analog RF signal generated at a local  
2      system, comprising:

3           generating a sample clock having an associated sample rate;

4           receiving and converting the analog RF signal into a first data stream of digitized RF  
5      data samples at the sample rate determined by the sample clock;

6           providing a second data stream, where second data stream is provided at a rate that is  
7      less than the sample rate;

8               combining the first data stream and second data stream to generate a combined data  
9       stream; and

10              converting the combined data stream into a serialized optical data signal for  
11       transmission over an optical fiber.

1       24.     The method of claim 23, including:

2               generating maintenance data indicative of an operational state of the return path  
3       transmitter and including the maintenance data in the second data stream.

1       25.     The method of claim 24, including:

2               locally storing data including at least one of a serial number, model number, date of  
3       manufacture, software revision number and hardware revision number of the transmitter, and  
4       including in the second data stream at least a portion of the locally stored data.

1       26.     The method of claim 23, including:

2               receiving a third data stream from a source external to the return path transmitter, the  
3       third data stream having a data rate of at least 5 Mb/s; and  
4               merging the first and third data streams into a merged data stream;  
5               wherein the combining includes combining the merged data stream and second data  
6       stream to generate the combined data stream.

1       27.     The method of claim 26, including

2               buffering the merged data stream in a first memory device;  
3               buffering the second data stream in a second memory device;  
4               generating an output clock having an associated output frequency;  
5               monitoring a fullness level of the first memory device; and  
6               outputting data stored in the first memory device in a first mode when the fullness  
7       level of the first memory device is more than a predefined threshold level, and outputting data  
8       stored in the first memory device and data stored in the second memory device in a second  
9       interleaved mode when the fullness level of the first memory device is less than the  
10      predefined threshold level.

1       28.     The method of claim 23, including

2 buffering the first data stream in a first memory device;  
3 buffering the second data stream in a second memory device;  
4 generating an output clock having an associated output frequency;  
5 monitoring a fullness level of the first memory device; and  
6 outputting data stored in the first memory device in a first mode when the fullness  
7 level of the first memory device is more than a predefined threshold level, and outputting data  
8 stored in the first memory device and data stored in the second memory device in a second  
9 interleaved mode when the fullness level of the first memory device is less than the  
10 predefined threshold level.

1 29. The method of claim 23, including:  
2 sampling data from the first data stream to generate a set of sampled RF data and  
3 including the sampled RF data in the second data stream.

1 30. The method of claim 23, wherein:  
2 the second data stream is provided intermittently; and  
3 inserting padding words into the combined data stream so as to maintain the  
4 combined data stream at a fixed data rate.

1 31. A method transmitting data representing first and second analog RF signals generated  
2 at first and second local systems, comprising:  
3 generating a sample clock having an associated sample rate;  
4 receiving and converting the first and second respective analog RF data signals into  
5 first and second data streams of digitized RF data samples at the sample rate determined by  
6 the sample clock;  
7 providing a third data stream;  
8 combining the first, second and third data streams to generate a combined data stream;  
9 and  
10 converting the combined data stream into a serialized optical data signal for  
11 transmission over an optical fiber.

1 32. The method of claim 31, including:  
2 buffering the first data stream in a first memory device;

3 buffering the second data stream in a second memory device;  
4 buffering the third data stream in a third memory device;  
5 generating an output clock having an associated output frequency;  
6 monitoring a fullness level of the first memory device; and  
7 outputting data stored in the first and second memory devices in a first mode when the  
8 fullness level of the first memory device is more than a predefined threshold level, and  
9 outputting data stored in the first and second memory devices and data stored in the third  
10 memory device in a second interleaved mode when the fullness level of the first memory  
11 device is less than the predefined threshold level.

1 33. The method of claim 32, wherein the providing includes receiving the third data  
2 stream from a digital data source external to the return path transmitter, the third data stream  
3 having a data rate of at least 5 Mb/s.

1 34. A method transmitting data representing an analog RF signal generated at a local  
2 system, comprising:  
3 receive a digital optical signal and generate therefrom a first digitized RF data stream  
4 and a sample clock having an associated sample rate;  
5 receiving and converting the analog RF signal into a second digitized RF data stream  
6 of digitized RF data samples at a rate determined by the sample clock;  
7 mathematically summing the first and second digitized RF data streams so as to  
8 generate a third digitized RF data stream; and  
9 converting an output data stream into a serialized optical data signal for transmission  
10 over an optical fiber, the output data stream including the third digitized RF data stream.

1 35. The method of claim 34, including:  
2 demultiplexing data within the received digital optical signal into a first digitized RF  
3 data stream and a first non-RF data stream;  
4 receiving a second non-RF data stream from a digital data source external to the  
5 return path transmitter, the second non-RF data stream having a data rate of at least 5 Mb/s;  
6 extracting a portion of the first non-RF data stream and replacing the extracted portion  
7 of the first non-RF data stream with the second non-RF data stream so as to generate a third  
8 non-RF data stream; and

9               combining the third digitized RF data stream and the third non-RF data stream and  
10          generate a combined data stream;  
11               wherein the output data stream includes the combined data stream.

1       36.     An optical signal receiver comprising:  
2               a signal receiver for receiving an digital input signal and recovering therefrom a  
3               digital data stream and an associated first clock having an associated first clock rate;  
4               a memory device configured to store the data stream at a rate corresponding to the  
5               first clock rate;  
6               a clock generator for generating a second clock having an associated second clock  
7               rate, wherein the clock generator is configured to adjust the second clock rate in accordance  
8               with a clock control signal;  
9               logic for reading data from the memory device at a rate corresponding to the second  
10          clock rate and for generating a fullness signal that indicates whether the memory device is  
11          more full than a predefined threshold fullness level; and  
12               a clock speed adjusting circuit configured to generate the clock control signal in  
13          accordance with the fullness signal.

1       37.     The receiver of claim 36, wherein the clock generator includes a voltage controlled  
2          crystal oscillator and the clock control signal is a voltage signal.

1       38.     An optical signal receiver comprising:  
2               a signal receiver for receiving an digital input signal and recovering therefrom a  
3               digital data stream and an associated first clock having an associated first clock rate, the  
4               digital data stream including a first data stream having an associated first data rate and a  
5               second data stream having an associated second data rate that is different from the first data  
6               rate; the first data stream comprising a sequence of data frames, each data frame representing  
7               a sequence of samples of an RF signal;  
8               a first memory device configured to store the first data stream;  
9               a second memory device configured to store the second data stream;  
10              a demultiplexer for receiving the digital data stream, detecting boundaries of the data  
11          frames in the first data stream and storing the data frames in the first memory device,

12 identifying data in the digital data stream comprising the second data stream and storing the  
13 second data stream in the second memory device;  
14       a clock generator for generating a local sample clock having an associated sample  
15       clock rate;  
16       logic circuitry for reading data from the first memory device at a rate corresponding to  
17       the sample clock rate so as to regenerate the sequence of samples of the RF signal represented  
18       by the sequence of data frames comprising the first data stream; and  
19       a digital to analog converter for converting the regenerated sequence of samples at the  
20       sample clock rate into an analog signal comprising a regenerated version of the RF signal.

1 39. The receiver of claim 38, wherein  
2       the logic circuitry is configured to generate a fullness signal that indicates whether the  
3       first memory device is more full than a predefined threshold fullness level;  
4       the clock generator is configured to adjust the sample clock rate in accordance with a  
5       clock control signal; and  
6       the receiver includes a clock speed adjusting circuit configured to generate the clock  
7       control signal in accordance with the fullness signal.

1 40. The receiver of claim 38, wherein the logic circuitry is configured to read data from  
2       the second memory device and transmit the data read from the second memory device to a  
3       digital data device.

1 41. The receiver of claim 40, wherein the digital data device is a data processor.

1 42. The receiver of claim 40, wherein the digital data device is coupled to a network  
2       router for routing data packets in the second data stream.

1 43. An optical signal receiver comprising:  
2       a signal receiver for receiving an digital input signal and recovering therefrom a  
3       digital data stream and an associated first clock having an associated first clock rate, the  
4       digital data stream including first, second and third data streams, the first data stream  
5       comprising a first sequence of first data frames, each first data frame representing a sequence  
6       of samples of a first RF signal, the second data stream comprising a second sequence of

7 second data frames, each second data frame representing a sequence of samples of a second  
8 RF signal;  
9       a first memory device configured to store the first data stream;  
10      a second memory device configured to store the second data stream;  
11      a third memory device configured to store the third data stream;  
12      a demultiplexer for receiving the digital data stream, detecting boundaries of the first  
13 data frames in the first data stream and of the second data frames in the second data stream  
14 and storing the first data frames in the first memory device and the second data frames in the  
15 second memory device, identifying data in the digital data stream comprising the third data  
16 stream and storing the third data stream in the third memory device;  
17      a clock generator for generating a local sample clock having an associated sample  
18 clock rate;  
19      logic circuitry for simultaneously reading data from the first and second memory  
20 devices at a rate corresponding to the sample clock rate so as to regenerate the sequence of  
21 samples of the first RF signal represented by the sequence of first data frames comprising the  
22 first data stream and the sequence of samples of the second RF signal represented by the  
23 sequence of second data frames comprising the second data stream; and  
24      a first digital to analog converter for converting the regenerated sequence of samples  
25 of the first RF signal at the sample clock rate into an analog signal comprising a regenerated  
26 version of the first RF signal; and  
27      a second digital to analog converter for converting the regenerated sequence of  
28 samples of the second RF signal at the sample clock rate into an analog signal comprising a  
29 regenerated version of the second RF signal.

1     44.   The receiver of claim 43, wherein the logic circuitry is configured to read data from  
2 the third memory device and transmit the data read from the third memory device to a digital  
3 data device.

4     45.   An optical signal receiver comprising:  
5        a signal receiver for receiving an digital input signal and recovering therefrom a  
6 digital data stream and an associated first clock having an associated first clock rate, the  
7 digital data stream including a first data stream having an associated first data rate and a  
8 second data stream having an associated second data rate that is different from the first data

9 rate; the first data stream comprising a sequence of data frames, each data frame representing  
10 a sequence of summed samples of a plurality of RF signals, each summed sample comprising  
11 a mathematical sum of samples of a plurality of distinct RF signals;  
12       a first memory device configured to store the first data stream;  
13       a second memory device configured to store the second data stream;  
14       a demultiplexer for receiving the digital data stream, detecting boundaries of the data  
15 frames in the first data stream and storing the data frames in the first memory device,  
16 identifying data in the digital data stream comprising the second data stream and storing the  
17 second data stream in the second memory device;  
18       a clock generator for generating a local sample clock having an associated sample  
19 clock rate;  
20       logic circuitry for reading data from the first memory device at a rate corresponding to  
21 the sample clock rate so as to regenerate the sequence of summed samples of the plurality of  
22 RF signals represented by the sequence of data frames comprising the first data stream; and  
23       a digital to analog converter for converting the regenerated sequence of samples at the  
24 sample clock rate into an analog signal comprising a regenerated version of the plurality of  
25 RF signals superimposed on each other.

1       46. The receiver of claim 45, further including a cable modem termination system  
2 (CMTS) coupled to the digital to analog converter for receiving the analog signal and  
3 reconstructing therefrom digital messages encoded within each of the plurality of RF signals.

1       47. An optical signal receiver comprising:  
2       a signal receiver for receiving an digital input signal and recovering therefrom a  
3 digital data stream and an associated first clock having an associated first clock rate, the  
4 digital data stream including first and second data streams, the first data stream comprising a  
5 first sequence of first data frames, each first data frame representing a sequence of samples of  
6 a first RF signal, the second data stream comprising a second sequence of second data frames,  
7 each second data frame representing a sequence of samples of a second RF signal;  
8       a first memory device configured to store the first data stream;  
9       a second memory device configured to store the second data stream;  
10      a demultiplexor for receiving the digital data stream, detecting boundaries of the first  
11 data frames in the first data stream and of the second data frames in the second data stream

12 and storing the first data frames in the first memory device and the second data frames in the  
13 second memory device;

14 a clock generator for generating a local sample clock having an associated sample  
15 clock rate;

16 circuitry for simultaneously reading data from the first and second memory devices at  
17 a rate corresponding to the sample clock rate and for summing the data read from the first and  
18 second memories so as to generate a summed data stream signal; and

19 an analog converter for converting the summed data stream into an analog signal  
20 comprising regenerated versions of the first and second RF signals superimposed on each  
21 other.

1 48. A method of receiving a digital input signal, comprising:

2 receiving the digital input signal and recovering therefrom a digital data stream and an  
3 associated first clock having an associated first clock rate;

4 storing the data stream in a memory device at a rate corresponding to the first clock  
5 rate;

6 generating a second clock having an associated second clock rate, and adjusting the  
7 second clock rate in accordance with a clock control signal;

8 reading data from the memory device at a rate corresponding to the second clock rate;

9 generating a fullness signal that indicates whether the memory device is more full  
10 than a predefined threshold fullness level; and

11 generating the clock control signal in accordance with the fullness signal.

1 49. The method of claim 48, wherein the second clock is generated using a voltage  
2 controlled crystal oscillator and the clock control signal is a voltage signal.

1 50. A method of receiving a digital input signal, comprising:

2 receiving an digital input signal and recovering therefrom a digital data stream and an  
3 associated first clock having an associated first clock rate, the digital data stream including a  
4 first data stream having an associated first data rate and a second data stream having an  
5 associated second data rate that is different from the first data rate; the first data stream  
6 comprising a sequence of data frames, each data frame representing a sequence of samples of  
7 an RF signal;

8           detecting boundaries of the data frames in the first data stream and storing the data  
9       frames in a first memory device, and identifying data in the digital data stream comprising the  
10      second data stream and storing the second data stream in a second memory device;  
11           generating a local sample clock having an associated sample clock rate;  
12           reading data from the first memory device at a rate corresponding to the sample clock  
13      rate so as to regenerate the sequence of samples of the RF signal represented by the sequence  
14      of data frames comprising the first data stream; and  
15           converting the regenerated sequence of samples at the sample clock rate into an  
16      analog signal comprising a regenerated version of the RF signal.

1       51.     The method of claim 50, including:  
2           generating a fullness signal that indicates whether the first memory device is more full  
3      than a predefined threshold fullness level;  
4           generating a clock control signal in accordance with the fullness signal; and  
5           adjusting the sample clock rate in accordance with the clock control signal.

1       52.     The method of claim 50, including reading data from the second memory device and  
2      transmitting the data read from the second memory device to a digital data device.

1       53.     The method of claim 52, wherein the digital data device is a data processor.

1       54.     The method of claim 52, wherein the digital data device is coupled to a network router  
2      for routing data packets in the second data stream.

1       55.     A method of receiving a digital input signal, comprising:  
2           receiving the digital input signal and recovering therefrom a digital data stream and an  
3      associated first clock having an associated first clock rate, the digital data stream including  
4      first, second and third data streams, the first data stream comprising a first sequence of first  
5      data frames, each first data frame representing a sequence of samples of a first RF signal, the  
6      second data stream comprising a second sequence of second data frames, each second data  
7      frame representing a sequence of samples of a second RF signal;  
8           detecting boundaries of the first data frames in the first data stream and of the second  
9      data frames in the second data stream and storing the first data frames in a first memory

10 device and the second data frames in a second memory device, and identifying data in the  
11 digital data stream comprising the third data stream and storing the third data stream in a third  
12 memory device;

13 generating a local sample clock having an associated sample clock rate;

14 simultaneously reading data from the first and second memory devices at a rate  
15 corresponding to the sample clock rate so as to regenerate the sequence of samples of the first  
16 RF signal represented by the sequence of first data frames comprising the first data stream  
17 and the sequence of samples of the second RF signal represented by the sequence of second  
18 data frames comprising the second data stream;

19 converting the regenerated sequence of samples of the first RF signal at the sample  
20 clock rate into an analog signal comprising a regenerated version of the first RF signal; and

21 converting the regenerated sequence of samples of the second RF signal at the sample  
22 clock rate into an analog signal comprising a regenerated version of the second RF signal.

1 56. The method of claim 55, including reading data from the third memory device and  
2 transmitting the data read from the third memory device to a digital data device.

3 57. A method of receiving a digital input signal, comprising:

4 receiving an digital input signal and recovering therefrom a digital data stream and an  
5 associated first clock having an associated first clock rate, the digital data stream including a  
6 first data stream having an associated first data rate and a second data stream having an  
7 associated second data rate that is different from the first data rate; the first data stream  
8 comprising a sequence of data frames, each data frame representing a sequence of summed  
9 samples of a plurality of RF signals, each summed sample comprising a mathematical sum of  
10 samples of a plurality of distinct RF signals;

11 detecting boundaries of the data frames in the first data stream and storing the data  
12 frames in a first memory device, and identifying data in the digital data stream comprising the  
13 second data stream and storing the second data stream in a second memory device;

14 generating a local sample clock having an associated sample clock rate;

15 reading data from the first memory device at a rate corresponding to the sample clock  
16 rate so as to regenerate the sequence of summed samples of the plurality of RF signals  
17 represented by the sequence of data frames comprising the first data stream; and

18           converting the regenerated sequence of samples at the sample clock rate into an  
19       analog signal comprising a regenerated version of the plurality of RF signals superimposed  
20       on each other.

1       58.     The method of claim 57, further including processing the analog signal with a cable  
2       modem termination system (CMTS) so as to reconstruct therefrom digital messages encoded  
3       within each of the plurality of RF signals.

1       59.     A method of receiving a digital input signal, comprising:  
2           receiving an digital input signal and recovering therefrom a digital data stream and an  
3       associated first clock having an associated first clock rate, the digital data stream including  
4       first and second data streams, the first data stream comprising a first sequence of first data  
5       frames, each first data frame representing a sequence of samples of a first RF signal, the  
6       second data stream comprising a second sequence of second data frames, each second data  
7       frame representing a sequence of samples of a second RF signal;  
8           detecting boundaries of the first data frames in the first data stream and of the second  
9       data frames in the second data stream and storing the first data frames in the first memory  
10      device and the second data frames in the second memory device;  
11          generating a local sample clock having an associated sample clock rate;  
12          simultaneously reading data from the first and second memory devices at a rate  
13       corresponding to the sample clock rate and summing the data read from the first and second  
14       memories so as to generate a summed data stream signal; and  
15          converting the summed data stream into an analog signal comprising regenerated  
16       versions of the first and second RF signals superimposed on each other.